AMENDMENTS TO THE CLAIMS

Please amend claims 1-18 and add new claims 19-27 as shown in the LISTING OF CLAIMS below. The LISTING OF CLAIMS will replace all prior versions, and listings, of claims in the present application.

LISTING OF CLAIMS

Sub C1

1. (Currently Amended) A method for maintaining translation lookaside buffer ("TLB") coherency in a computer system having a plurality of processors, each of the [[said]] processors having an associated TLB for storing [[an]] address translation data, the system having a main communication network coupled to the plurality of processors, said method comprising:

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accessing a virtual address in an [[said]] associated TLB of one of the plurality of processors;

locating an associated physical address corresponding to said virtual address;

performing an operation on the associated TLB;

generating [[sending]] a TLB message in response to the operation performed on the associated TLB, if (a) ~~from one of said plurality of processors to said main communication network if (1)~~ a first entry was input into the associated TLB when the [[said]] corresponding associated physical address was not located; (b) [[(2)]] a second entry associated with the [[within said]] corresponding associated physical address was moved to another location within the [[said]] computer system; or (c) the [[(3) said]] second entry was removed; and

sending the [[said]] TLB message to the plurality of processors other than the processor associated with the TLB on which the operation was performed via the [[from said]] main communication network ~~to said plurality of processors~~.

2. (Currently Amended) The method in accordance with [[of]] claim 1, wherein the [[said]] TLB message [[further]] comprises:

a request for a read access to the [[said]] first entry to add the [[said]] address translation data into the [[said]] associated TLB.

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3. (Currently Amended) The method in accordance with [[of]] claim 1, wherein the [[said]] TLB message [[further]] comprises:

a request for a write access to the [[said]] second entry [[and]] to modify, remove, or invalidate all copies of the [[said]] second entry in the [[each of said]] associated TLB of each of the [[in said]] plurality of processors.

4. (Currently Amended) The method in accordance with [[of]] claim 1, further comprising:

comparing the [[said]] first entry with the [[said]] address translation data in the [[said]] associated TLB and informing the [[said]] associated TLB if the [[said]] first entry affects said address data stored therein.

5. (Currently Amended) The method in accordance with [[of]] claim 4, further comprising: [[comprising]]

adding the [[said]] address translation data in the [[said]] first entry into the [[said]] associated TLB in each of the [[said]] plurality of processors.

6. (Currently Amended) The method in accordance with [[of]] claim 1, further comprising:

comparing the [[said]] second entry with the [[said]] address data in the [[said]] associated TLB and informing the [[said]] associated TLB if the [[said]] second entry affects the [[said]] address data stored therein.

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7. (Currently Amended) The method in accordance with [[of]] claim 6, further comprising: [[comprising]]

invalidating the [[said]] address translation data in the [[said]] second entry in the [[said]] associated TLB in each of the [[said]] plurality of processors.

8. (Currently Amended) A program storage device readable by a machine, tangibly embodying a program of instructions executable by the machine to perform a method for maintaining translation lookaside buffer ("TLB") [[TLB]] coherency in a computer system having a plurality of processors, each of said processors having an associated TLB for storing [[an]] address translation data, the system having a main communication network coupled to the plurality of processors, said method comprising:

accessing a virtual address in an [[said]] associated TLB of one of the plurality of processors;

locating an associated physical address corresponding to said virtual address;

performing an operation on the associated TLB;

generating [[sending]] a TLB message in response to the operation performed on the associated TLB, if (a) ~~from one of said plurality of processors to said main communication network if (1)~~ a first entry was input into the associated TLB when the [[said]] corresponding associated physical address was not located; (b) [[(2)]] a second entry associated with the [[within said]] corresponding associated physical address was moved to another location within the [[said]] computer system; or (c) the [[(3) said]] second entry was removed; and

sending the [[said]] TLB message to the plurality of processors other than the processor associated with the TLB on which the operation was performed via the [[from said]] main communication network ~~to said plurality of processors~~.

9. (Currently Amended) An electronic data processing apparatus capable of maintaining translation lookaside buffer ("TLB") coherency, said apparatus comprising:

a plurality of processors;

a plurality of TLBs, each of said plurality of TLBs being connected to and associated with a respective processor of said plurality of processors;

an interconnect network having a plurality of independent paths, each of said plurality of processors distributed among said [[said]] plurality of independent paths, [[with each]] said plurality of processors being interconnected [processor connecting] to each other via corresponding one of said plurality of independent paths; and

a TLB message generator provided for each of the plurality of processors, said TLB message generator adapted to determine an accessed [[for accessing a]] data address

and generate and transmit ~~transmitting~~ a TLB message on corresponding one of said plurality of independent paths.

10. (Currently Amended) The apparatus in accordance with [[of]] claim 9, wherein the [[said]] TLB message [[further]] comprises:

a read access message if the [[said]] accessed data address is inputted into an [[said]] associated TLB.

11. (Currently Amended) The apparatus in accordance with [[of]] claim 9, wherein the [[said]] TLB message [[further]] comprises:

a write access message if the [[said]] accessed data address modifies, removes, or invalidates the [[said]] address translation data in an [[said]] associated TLB.

12. (Currently Amended) A system for maintaining translation lookaside buffer ("TLB") [[TLB]] coherency in a computer system[[, comprising:]] including a plurality of processors[[;]] and a plurality of TLBs, each of said plurality of TLBs being connected to and associated with a respective processor of said plurality of processors, said system comprising:[[;]]

an interconnect network having a plurality of independent paths, each of said plurality of processors distributed among said plurality of independent paths, said plurality of processors being interconnected to each other via corresponding ~~with each processor and its associated TLB connecting to~~ one of said plurality of independent paths;

means for accessing ~~performing an access to~~ a data address from one of the [[its said]] associated TLBs [[TLB]];

a TLB message generator for generating a TLB message in response to an operation performed on said one of the associated TLBs; and

means for transmitting the [[said]] TLB message and the accessed data address to each processor associated with a TLB other than the TLB on which the operation was performed via corresponding one of the plurality of independent paths ~~said access data to a main communication network~~.

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13. (Currently Amended) The system in accordance with [[of]] claim 12, further comprising: [[comprising]]

means for ~~transmitting said TLB message and said access data on said plurality of independent paths and~~ comparing the [[said]] accessed data address with [[an]] address translation data [[of the information]] stored in each of the [[said]] plurality of TLBs, the [[said]] TLB message being capable of informing each of the [[said]] plurality of TLB if the accessed [[said access]] data address affects the access translation data stored in the TLB [[therein]].

14. (Currently Amended) The system in accordance with [[of]] claim 12, further comprising: [[comprising]]

means for adding the accessed [[said access]] data address into the [[said]] associated TLB in each of the [[said]] plurality of processors.

15. (Currently Amended) The system in accordance with [[of]] claim 12, further comprising: [[comprising]]

means for invalidating the [[said]] address translation data in the [[said]] associated TLB in each of the [[said]] plurality of processors.

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16. (Currently Amended) The system in accordance with [[of]] claim 12, further comprising: [[comprising]]

means for moving the [[said]] address translation data in the [[said]] associated TLB in each of the [[said]] plurality of processors to another part of the computer system.

17. (Currently Amended) The system in accordance with [[of]] claim 12, wherein the TLB message further comprises:

a read access message if the [[said]] accessed data address is inputted into the [[said]] associated TLB.

18. (Currently Amended) The system in accordance with [[of]] claim 12, wherein the TLB message further comprises:

a write access message if the [[said]] accessed data invalidates the [[said]] address translation data in the [[said]] associated TLB.

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19. (New) The method in accordance with claim 1, wherein the main communication network includes:

an interconnect network having a plurality of independent paths, the plurality of processors being interconnected to each other via corresponding one of the plurality of independent paths.

20. (New) An apparatus for maintaining translation lookaside buffer ("TLB") coherency in a computer system including a plurality of processors, each of the plurality of processors having an associated TLB for storing address translation data, said apparatus comprising:

means for accessing a virtual address in an associated TLB of one of the plurality of processors;

means for locating an associated physical address corresponding to said virtual address;

means for generating a TLB message in response to an operation performed on an associated TLB, if (a) a first entry was input into the associated TLB when the corresponding associated physical address was not located; (b) a second entry associated with the corresponding associated physical address was moved to another location within the computer system; or (c) the second entry was removed; and

means for transmitting the TLB message from the processor associated with the TLB on which the operation is performed to other processors of the plurality of processors via plurality of independent paths.

21. (New) The apparatus in accordance with claim 20, wherein said means for transmitting comprises:

means for interconnecting each of the plurality of processors to one another via corresponding one of the plurality of independent paths.

22 (New) The apparatus in accordance with claim 20, wherein the TLB message comprises:

a request for a read access to the first entry to add the address translation data into the associated TLB.

23. (New) The apparatus in accordance with claim 20, wherein the TLB message comprises:

a request for a write access to the second entry to modify, remove, or invalidate all copies of the second entry in the associated TLB of each of the plurality of processors.

24. (New) The apparatus in accordance with claim 20, further comprising:

means for comparing the first entry with the address translation data in the associated TLB and for informing the associated TLB if the first entry affects said address data stored therein.

25. (New) The apparatus in accordance with claim 24, further comprising:

means for adding the address translation data in the first entry into the associated TLB in each of the plurality of processors.

26. (New) The apparatus in accordance with claim 20, further comprising:

means for comparing the second entry with the address data in the associated TLB and for informing the associated TLB if the second entry affects the address data stored therein.

27. (New) The apparatus in accordance with claim 26, further comprising:

means for invalidating the address translation data in the second entry in the associated TLB in each of the plurality of processors.